DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute Affiliated to VTU, Belagavi, Approved by AICTE and UGC, Accredited by NAAC with 'A' Grade)

Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560111

Department of Electronics and Communication Engineering

Faculty Development Programme on
"A Learning on Complete Life Cycle of VLSI Chip Making"
10th to 14th March 2025
Schedule

				11:00 to 11:30 Tea Break			1:00 to 2:00 Lunch Break	3:30 to 4:00 Tea Break
Day 1 **10th March 2025**	9:30 to 10:15 Inauguration by Principal, DSCE and HOD, ECE, DSCE **and** Dr KD Nayak, Dr Ravi Meduri and Dr MH Kori (IMAPS)	10:15 to 10:40 Indian Semiconductor Industry Status and GOI Initiatives by Dr KD Nayak (former DG DRDO)	10:40 to 11:00 Semiconductors for Defence Applications - Opportunities and Challenges by Dr Ravi Meduri (Director STARC/DRDO)	11:30 to 12:00 Importance of the FDP and way forward *(+ new applications)* by Dr MH Kori (former Technical Director Alcatel Lucent)	12:00 to 12:15 IMAPS activities and Membership Drive by IMAPS Rep.	12:15 to 1:00 Choice of Materials Si, GaAs, GaN **and** Brief detailing on VLSI Design by Dr Dinesha (Sr Prof. DSCE)	2:00 to 3:30 Interdisciplinary Research Overview of Micro& Nano Technology by Dr Sabiha (Chief Technologist CeNSE, IISc Bangalore)	4:00 to 4:30 EDA Tools and Comparative Studies (by TrueChip)

	9:30 to 11:00	11:00 to 11:30	11:30 to 1:00	1:00 to 2:00	200 to 3:30	3.30 to 4.00	4.00 to 5.00
Day 2 **11th March 2025**	Clean Room Requirements (+ ESD) by Jayaramu H.E. (Manager STARC)	Tea Break	Photolithography by B Bhattacharya (Deputy GM STARC)	Lunch Break	VLSI Fabrication (and Process Integration) by Dr Shalini Shrivastava (Visiting Research Fellow IISc Bangalore)	Tea Break	Future Research Trends in VLSI by Dr Kiran Gupta (Sr Prof. DSCE)
Day 3 **12th March 2025**	**Industrial Visit to SITAR/STARC and ITI Ltd.** (Start at 8:00 AM at DSCE)						
Day 4 **13th March 2025**	Advanced Semiconductor Packaging Technologies (Part I) by Dr Shankara Prasad (Prof. of Practice IIT Guwahati)	Tea Break	Advanced Semiconductor Packaging Technologies (Part II) and Packaging Future Trends by Dr Shankara Prasad	Lunch Break	Assembly, Testing and OSTA by Dr Veena Chakravarti (Sr. Prof)	Tea Break	VLSI Packaging/Mfg. Industry Perspective by Sharat D Kaul (Consultant Kaynes Semicon)
Day 5 **14th March 2025**	Qualification of VLSI and Microelectronic devices for aerospace and defence applications (Wafer level and Chip level) by Dr Gopal Sharma R Joshi (formerly Scientist ISRO, Prof CSST DSU)	Tea Break	Semiconductor Integrated Circuits Layout Design Protection SICLD Act 2000 by Dr YVS Lakshmi (IPR Consultant CDOT)	Lunch Break	Feedback Session <group exercises> and Way-Forward <making a bigger program for larger target audience>	Tea Break	Concluding Session and Certificate Distribution